New Readout Electronics for 3-D Position Sensitive CdZnTe/HgI_2 Detector Arrays

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***Abstract*—The 4th-generation readout system based on VAS_UM/TAT4 ASICs for 3-D position sensitive CdZnTe/HgI_2 detector arrays has been developed and tested. Each VAS_UM/TAT4 chip is a 129-channel self-triggered monolithic Application Specific Integrated Circuit (ASIC). One 3-D position-sensitive detector module consists of one CdZnTe or HgI_2 gamma-ray spectrometer, and one VAS_UM/TAT4 ASIC mounted on a 2.2 cm $\times$ 2.2 cm front-end board. Each detector has an array of 11 by 11 pixel anodes fabricated on the anode surface with an area up to 2 cm $\times$ 2 cm. The detector and the front-end board are connected by three pairs of 42-pin connectors for easy assembly and component replacement. Up to nine detector modules can be plugged into a single motherboard to form a 3 by 3 detector array. The VAS_UM/TAT4 chip can read out both the amplitude of induced charge on each electrode and the electron drift time needed for reconstructing energy deposition and three-dimensional coordinates of each radiation interaction. Three different sets of VAS_UM/TAT4 chips with different dynamic ranges and shaping times were fabricated for gamma-ray spectroscopy in CdZnTe and HgI_2. These are the first ASIC readout systems that allow multiple 3-D position sensitive CdZnTe/HgI_2 detector modules to be tiled together, to achieve a detection volume greater than 50 cm^3 on a single detector plane. Multiple planes of detector arrays can be operated together to achieve more than 100 cm^3 detection volume on a single system. In this paper, the VAS_UM/TAT4 ASIC systems are described and their test results are reported.**

***Index Terms*—Array, CdZnTe, CZT, position sensitive, readout, spectrometer, three-dimensional (3-D).**

I. Introduction

With increasing demands on high resolution, high efficiency and room temperature operational gamma-ray spectrometers and imagers for nuclear non-proliferation and homeland security applications, wide band-gap semiconductors, such as CdZnTe and HgI_2, have gained more interests as promising candidates for these applications. Although many single-polarity charge-sensing techniques, such as those employing coplanar-grid [1], Frisch-grid [2], or simple pixellated anodes [3], [4], successfully mitigated the hole trapping problem and improved energy resolution on larger volume CdZnTe and HgI_2 detectors, material non-uniformity and electron trapping still degrade the energy resolution. As a result, energy resolution of large volume (with an area about 2 cm^2 and a thickness about 1 cm) CdZnTe detectors today typically stay above 2% FWHM at 662 keV.

The three-dimensional (3-D) position-sensitive technique using pixellated anodes has the ability to provide energy and 3-D coordinates of each individual gamma-ray interaction. Hence, a correction for material non-uniformity and electron trapping in 3-dimensions becomes feasible. The development of the 1st-generation and 2nd-generation 3-D position-sensitive CdZnTe spectrometers were reported in 1998 [5], [6] and 2003 [7], respectively. In 2004, we reported two 3-D position sensitive CdZnTe spectrometers coupled with the 3rd generation VAS3.1/TAT3 ASIC readout systems [8], [9]. Both systems utilized 1.5 cm $\times$ 1.5 cm $\times$ 1 cm CdZnTe crystals employing 11 by 11 pixellated anodes. One system achieved an energy resolution of 0.76%, and the other 0.93% FWHM at 662 keV for single-pixel events. With the capability of electron drift time measurement on the ASIC, these devices can also reconstruct multiple gamma-ray interaction events, which is important for high-energy gamma-ray detection [10] and Compton imaging [11], [12]. However, the detection efficiency of these systems is still too low for most applications due to the small 2.25 cm^3 sensitive volume.

In an effort to build hand-held 3-D position sensitive CdZnTe detectors with high detection efficiency, we have been collaborating with Gamma Medica-Ideas Inc. to develop the 4th-generation ASICs-VAS_UM/TAT4 and the readout system. The most significant improvement from the previous VAS3.1/TAT3 system is that the VAS_UM/TAT4 ASIC and the front-end board are miniaturized to closely match the size of the detector, thus multiple detector modules can be plugged on the motherboard to form an expandable detector array.

The basic configuration of the VAS_UM/TAT4 system is described and the preliminary test results of the readout electronics, such as gain, dynamic range, linearity and electronic noise, are reported and discussed.

II. The VAS_UM/TAT4 ASIC

The design of the VAS_UM/TAT4 ASIC was based on the proven VAS3.1/TAT3 ASIC chips. Their functions and major design architectures are the same [9]. The block diagrams of a single VAS_UM/TAT4 channel and the full ASIC chip are shown in Figs. 1 and 2. There are two major differences between the VAS_UM/TAT4 chip and VAS3.1/TAT3 chip set.

First, the VAS_UM/TAT4 chip has the charge amplitude sensing (VAS) and the electron drift time sensing (TAT) integrated inside one single chip while the VAS3.1/TAT3 chipset used two separate ASIC chips (one for charge sensing and the other for timing measurement).

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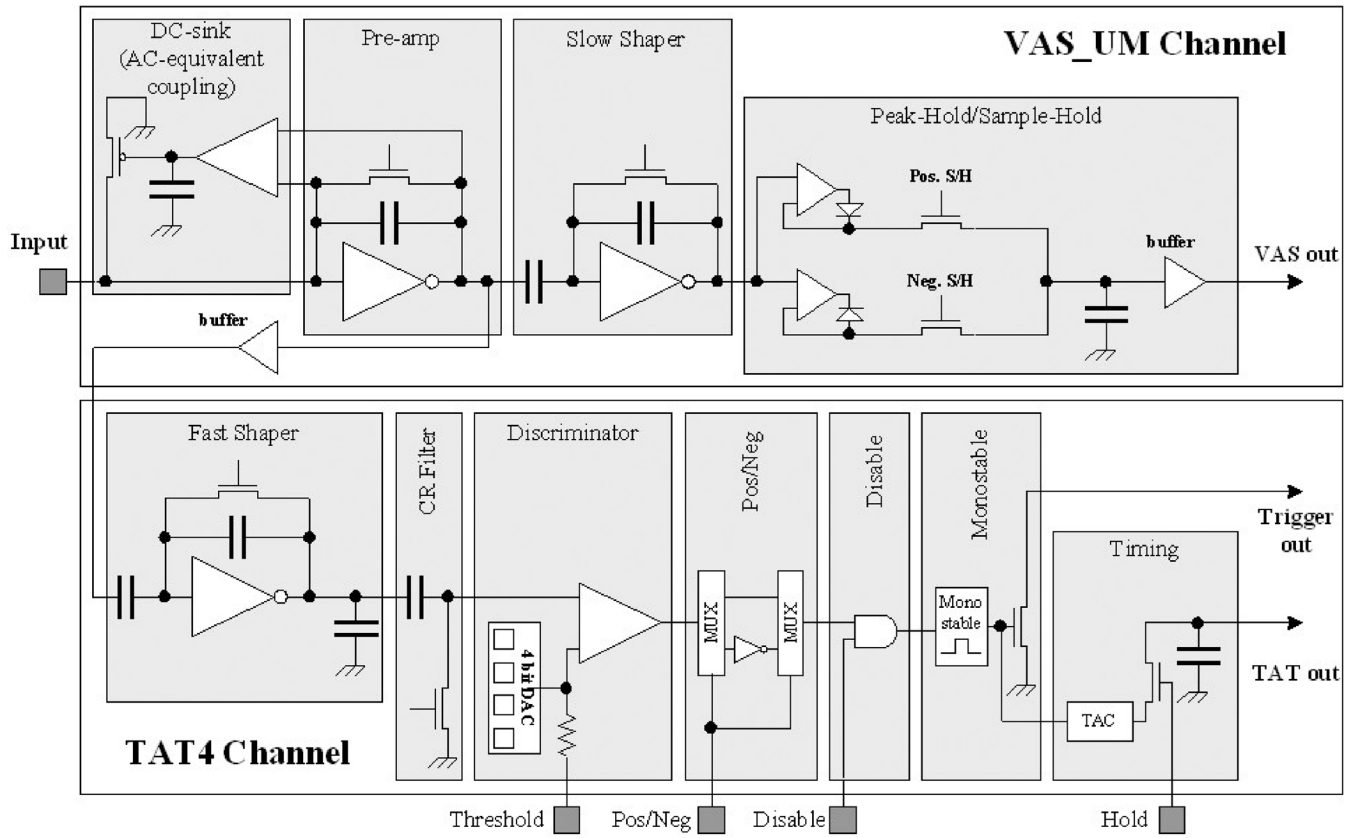

Fig. 1. Block diagram of a single VAS_UM/TAT4 channel.

Second, the VAS_UM/TAT4 chip has 129 channels so that only one chip is needed for one CdZnTe detector with 11 by 11 pixellated anodes, while four 32-channel VAS3.1/TAT3 chip pairs are needed for a detector having the same number of pixel anodes.

There are three different types of channels among the 129 channels on one VAS_UM/TAT4 ASIC. Five channels are designed to read out signals (positive charge) from the cathode and the anode grid, and are named "special" channels, while 123 channels are used to read out signals (negative charge) from the anode pixels and are called "normal" channels. The last channel is a "test" channel designed for two purposes. First, the charge amplitude measurement unit (VAS) of this channel does not have a stretch (peak-hold circuitry) so that the output waveform of the shaper can be directly monitored for diagnostic purpose. Second, the timing measurement unit (TAT) is replaced by an on-chip thermometer and is used to monitor and calibrate the temperature drift of the system.

Minimizing the changes to the previous successful ASIC design (VAS3.1/TAT3) to reduce the risk while trying to get the best performance, three different sets of VAS_UM/TAT4 chips were fabricated—the first set (VAS_UM1/TAT4) is for intermediate energy gamma-ray spectroscopy in CdZnTe with a dynamic range up to 1 MeV per channel. The second set (VAS_UM2/TAT4) is for higher-energy gamma-ray detection in CdZnTe for energy deposition of up to 3 MeV per channel and the third set (VAS_UM3/TAT4) is for HgI_2 gamma-ray spectrometers (up to 1 MeV per channel). The first two chips both have a shaping time of $\sim$1 μs, while the third chip has a shaping time of $\sim$6 μs to account for the slower drift of electrons in HgI_2. The choice of shaping times is based on experimental evaluation of 1 cm thick pixellated CdZnTe and HgI_2 detectors using standard NIM devices.

The ASIC chip was designed and fabricated by Gamma Medica-Ideas Inc. using 0.35 μm CMOS technology. The resulting die size is 9805 μm by 7890 μm and 725 μm thick, which makes it possible to be integrated on a small size front-end board.

III. Readout System Description

A readout system mainly consists of a motherboard (MOCA-9) and a digital readout board (CROB-16), as shown in Fig. 3. Up to nine detector modules (CdZnTe/HgI_2 detector coupled with the ASIC front-end board) can be plugged into the motherboard. The operation of the ASIC and the readout of the detectors are controlled by the motherboard. The digital readout board can accommodate up to four motherboards. A National Instruments digital I/O board (PCI-DIO32-HS) mounted inside a personal computer is used to communicate with the readout board.

A. Front-End Board

The integration of 129 VAS_UM/TAT channels into one ASIC chip has made it possible to reduce the dimensions of the front-end board, where the ASIC is mounted, from about 9 cm $\times$ 12 cm in a VAS3.1/TAT3 system to 2.2 cm $\times$ 2.2 cm in a

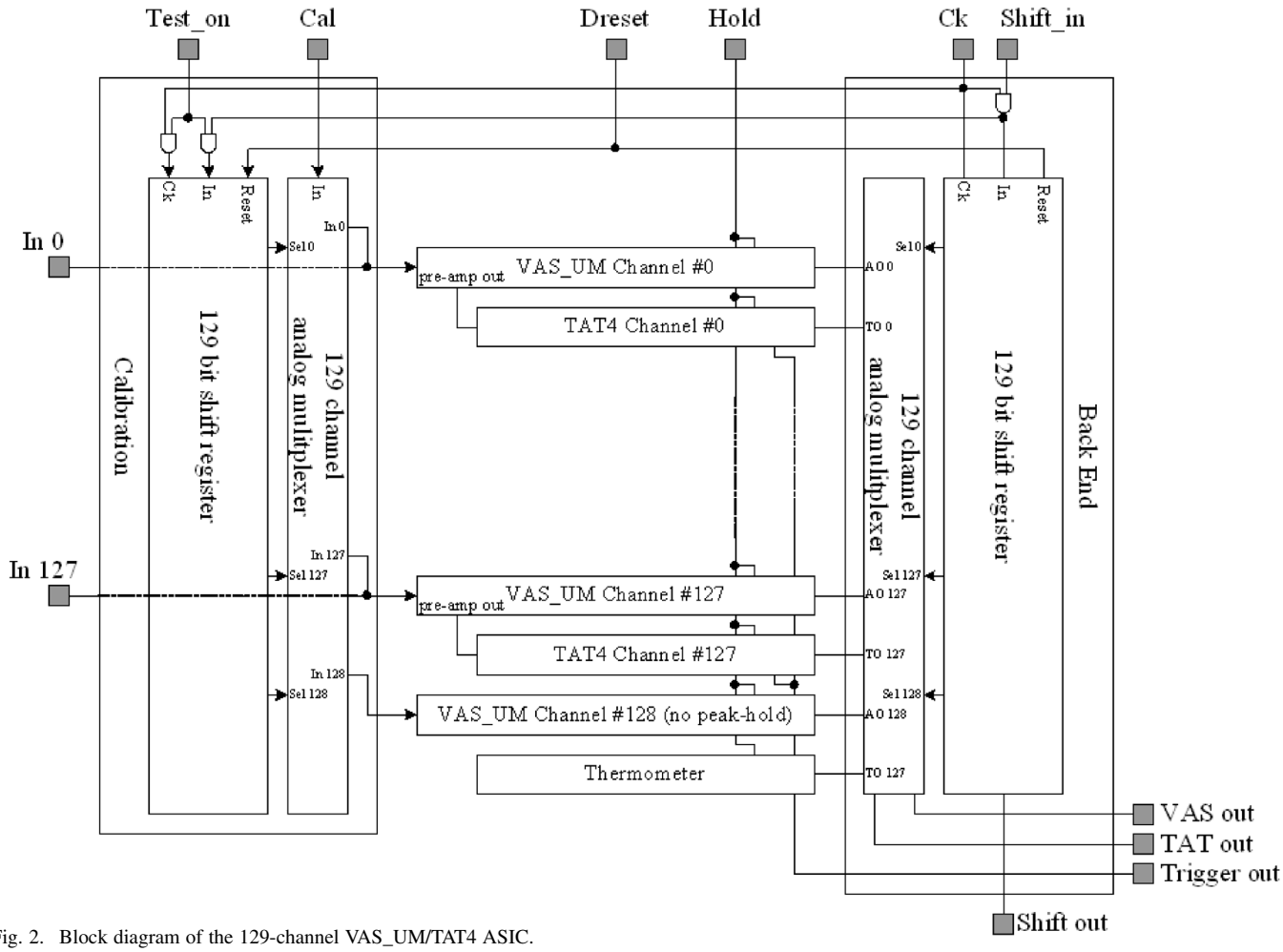

Fig. 2. Block diagram of the 129-channel VAS_UM/TAT4 ASIC.

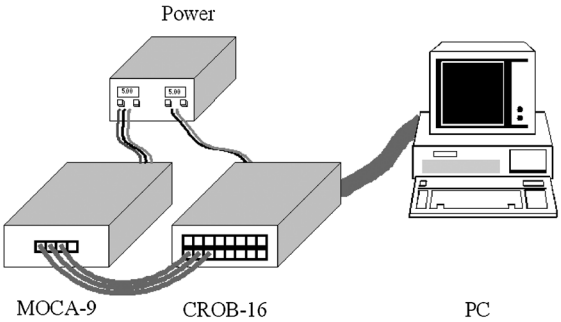

Fig. 3. The basic configuration of the 3-D position sensitive CdZnTe detector array system, mainly consisting the MOCA-9 (motherboard) and the CROB-16 (digital readout board).

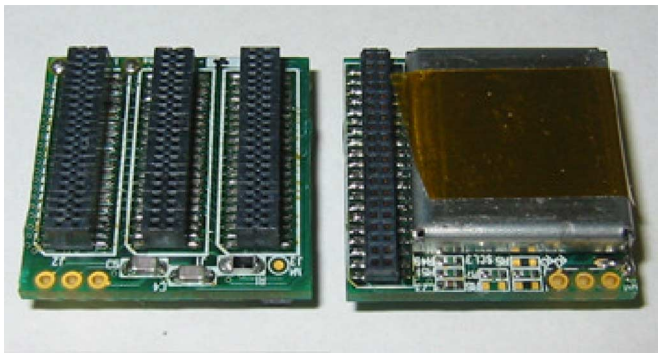

Fig. 4. Photos of the VAS_UM/TAT4 ASIC front-end board. Left: ASIC front-end board facing the detector substrate, three 42-pin 0.8 mm pitch connectors are used. Right: ASIC front-end board facing the motherboard (one 40-pin 1.0 mm pitch connector, the 129 channel VAS_UM/TAT4 ASIC is enclosed inside the heat-sink).

VAS_UM/TAT4 system. One VAS_UM/TAT4 chip is mounted on a front-end board (cf. Fig. 4) that can be connected to one 3-D CdZnTe or HgI_2 detector to form a detector module. There is a 40-pin 1.0 mm pitch connector on one side of the front-end board connecting the module to the motherboard. There are three 42-pin 0.8 mm pitch connectors on the other side of the front-end board connecting the board with the detector. The detector substrate has matching pins for these connectors.

B. Motherboard (MOCA-9)

A motherboard with six front-end boards installed is shown in Fig. 5. An array of 3 by 3 detector modules can be plugged into the rightmost region of the motherboard. The array is divided into three daisy chains with three detector modules in each chain. All channels of the three modules in the same chain are read out serially, while the three chains are read out in parallel. Each chain has two parallel outputs-one is the charge amplitude signal and the other is the timing signal.

There are six parallel 14-bit ADCs (400 kHz) in the middle of the motherboard right next to the detector modules. In the VAS3.1/TAT3 systems, the analog signals were sent through a two-meter long cable to a DAQ board inside the computer,

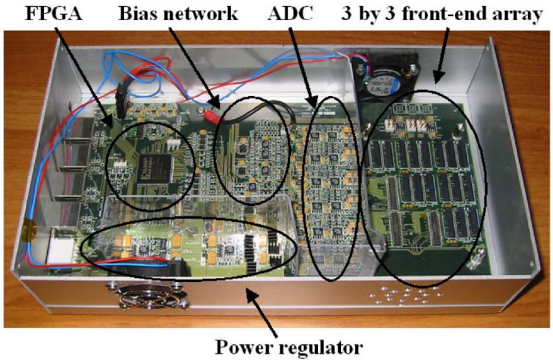

Fig. 5. Photo of the VAS_UM/TAT4 motherboard. The left parts are the on-board ADCs and digital control electronics. The right part is the 3 by 3 ASIC array. Six ASIC front-end boards are plugged in. No CdZnTe detector is connected.

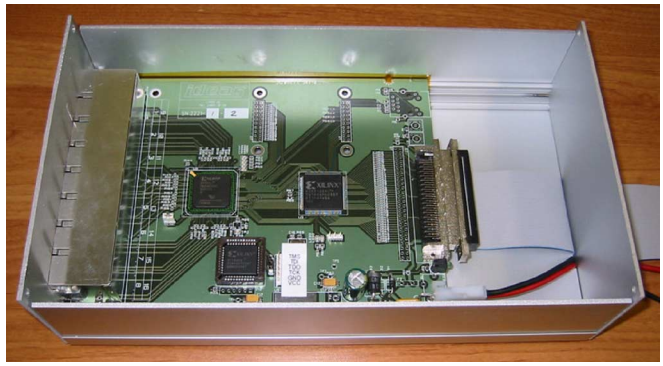

Fig. 6. Photo of the digital readout board (CROB-16).

where the signals were digitized. Additional noise might be introduced during the transmission. The new design is clearly more desirable since the ADCs are right next to the front-end board; analog signals are converted to digital signals much closer to detectors.

There are also several DACs on the motherboard, which generate some of the biases for the ASIC and the calibration pulse for diagnosis. This enables a complete digital control of the readout system from the computer.

The logic, which controls the ASICs, performs the data acquisition and transfers the digitized signal to the readout board, is implemented in a Field Programmable Gate Array (FPGA) visible on the left side of the motherboard. The current ASIC doesn't have sparse readout capability and no zero-suppressing function is programmed in the FPGA. For each triggered event, all 1161 channels of the 9 modules are readout and $\sim$4.5 KB data is transferred first to the readout board and then to the computer. The maximum trigger rate of $\sim$1000 counts per second is now limited by the data transfer bottleneck between the readout board and the computer. Future implementation of sparse readout either in ASIC or in FPGA could greatly increase the count rate capability.

Up to nine detector modules can be plugged into a single motherboard and work as a single 3D position sensitive CdZnTe spectrometer and imager with a sensitive volume up to 54 cm^3. Detector arrays on several motherboards can be operated together to achieve detection volume of more than 100 cm^3, or more if needed. This is the first system in which multiple 3D position sensitive CdZnTe detector modules can be tiled together to achieve high detection efficiency while preserving the energy resolution of a single detector.

C. Digital Readout Board (CROB-16) and Digital I/O Card

Due to budget and time constrains, although not completely necessary, a digital readout board (cf. Fig. 6) and a digital I/O card inside the computer are used in the current readout system. The digital readout board and the digital I/O card mainly work as the interface between the DAQ program and the motherboard. In the future, the FPGA on the motherboard can be programmed to perform all the work and communicate with the computer through standard interface such as Ethernet or USB.

TABLE I
ELECTRONIC NOISE OF THE THREE TYPES OF ASICS

	VAS_UM1	VAS_UM2	VAS_UM3
Special channel	5.0 keV FWHM (426 e^- rms)	6.3 keV FWHM (536 e^- rms)	7.6 keV FWHM (647 e^- rms)
Normal channel	4.0 keV FWHM (340 e^- rms)	5.2 keV FWHM (443 e^- rms)	5.8 keV FWHM (494 e^- rms)

IV. PERFORMANCE MEASUREMENTS

The DAQ program can digitally control the motherboard to generate an on-board calibration pulse being injected into one specific ASIC channel. Unfortunately, the calibration pulse has a much higher noise than expected due to some unknown noise pickup on its way from the DAC output to the ASIC input. Therefore the calibration pulse cannot be used to evaluate the electronic noise of the readout system.

The performance of VAS_UM/TAT4 ASICs has been mainly studied by injecting an external test pulse through a coaxial cable and a 3-pF capacitor directly into the ASIC input sockets.

A. Electronic Noise and Common Mode Noise

The electronic noise was estimated by measuring the FWHM of the test pulse peak. The results of the electronic noise from typical channels of three different types of ASICs are listed in Table I. Considering the possible noise pickup in the test pulse, the true electronic noise should be lower than the listed values. Therefore, the electronic noise of the VAS_UM1 system is better than what was measured from the VAS3.1 system ($\sim$5 keV FWHM for normal channels) using the same method. The electronic noise of the VAS_UM2 system is only slightly higher than the VAS_UM1 system while it has dynamic range twice as large. The electronic noise of the VAS_UM3 system is the highest among the three ASICs. This may be partly due to its longer shaping time of 6 μs. This chip is our first try to make an ASIC for pixellated HgI_2 and it has not been fully optimized and tested before delivery due to budget constrains.

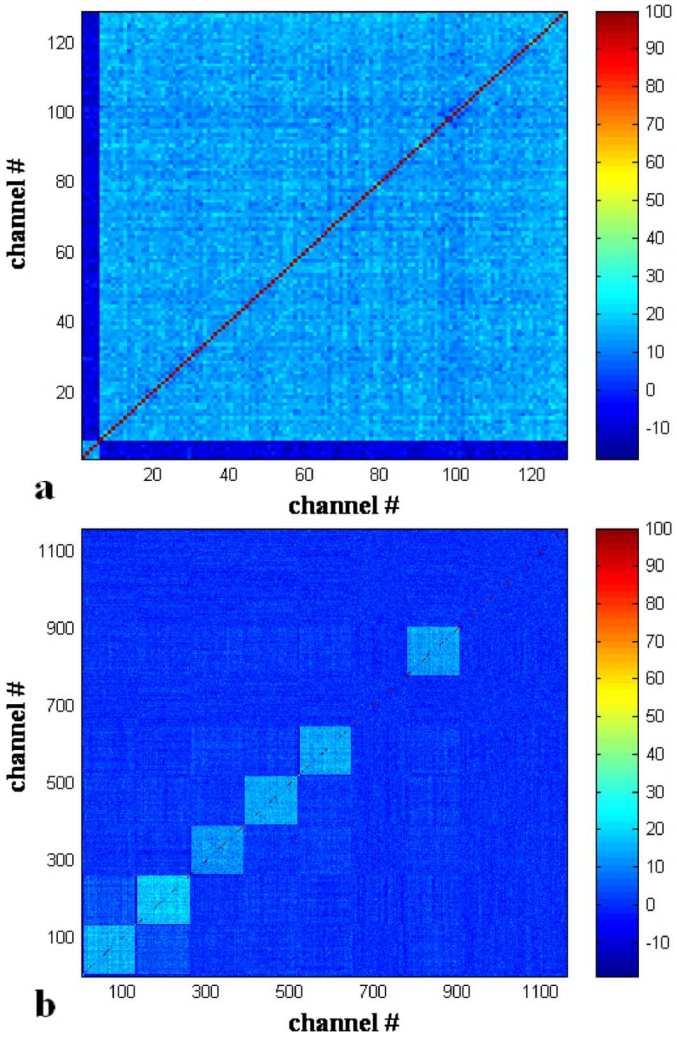

Fig. 7. Common mode noise in the VAS_UM/TAT4 readout system. (a). Pedestal fluctuation correlation among all 129 channel VAS signals in one ASIC. (b). Pedestal fluctuation correlation among all 1161 channel VAS signals in the whole system. Only 6 ASICs were plugged in the motherboard.

Common mode noise is a well-known problem in such multiple-channel analog-digital hybrid systems, and is usually an indication of shielding and grounding problems. The common mode noise of the VAS_UM/TAT4 readout system was studied by calculating the correlations between the pedestal fluctuations among the VAS signals of all channels in one ASIC [cf. Fig. 7(a)] and of all channels in the whole system [cf. Fig. 7(b)]. Fig. 7(a) shows that the VAS signals of all channels in one ASIC chip have common mode noise. We can clearly see that all normal channels have some correlation and all special channels have some correlation, but there is no correlation between these two kinds of channels. Fig. 7(b) shows that the common mode noise is restricted within each chip (each of the six block represents an ASIC front-end board plugged in the motherboard). There is no cross chip common mode noise. The common mode noise in VAS_UM systems is higher than that of the VAS_3.1 system (almost no such noise), but much lower than the second-generation VAS_2 system. The same measurement was applied to the TAT (timing) output signals of all channels and no common mode noise was observed.

TABLE II
DYNAMIC RANGES OF THE SPECIAL CHANNEL AND NORMAL CHANNEL FOR THE THREE TYPES OF ASICS

	VAS_UM1	VAS_UM2	VAS_UM3
Special channel	1.2 MeV (38 fC)	1.9 MeV (61 fC)	2.0 MeV (64 fC)
Normal channel	1.6 MeV (51 fC)	2.6 MeV (83 fC)	>3.0 MeV (96 fC)

B. Dynamic Range and Linearity

The dynamic ranges and linearity of special channels and normal channels for the three types of ASICs were studied by injecting calibration pulses with varying pulse amplitude into the ASIC channels. The results are summarized in Table II and Fig. 8, respectively.

The dynamic range of the VAS_UM1 ASIC meets the design goal. But the VAS_UM2 ASIC has lower than expected dynamic range especially in the special channel. The ASIC itself should have a dynamic range up to 3 MeV according to the test report of Ideas. The deficit is probably caused by the saturation while converting the ASIC output current to voltage signal on the motherboard. The dynamic ranges of the VAS_UM3 ASIC are much higher than expected, which also means the gain on the ASIC is lower than expected. This may be another reason why the VAS_UM3 chip has the highest electronic noise among the three types of ASIC.

Linearity is a key factor in reconstruction of multiple-pixel events. Before the signals from multiple pixels can be added together, the non-linearity in the signal must be corrected. All channels in all three ASICs showed some non-linearity, especially in the VAS_UM3 system. The special channels have better linearity than the normal channels. As long as the relation between the input and the output is smooth and stable, the non-linearity can be calibrated using different gamma-ray energies or using calibration pulses.

C. Pedestal and Gain Stability

The stability of the readout system was studied by injecting a 662 keV equivalent external test pulse into one ASIC channel and monitoring the pedestal and output of this channel over 24 hours. The results are shown in Fig. 9. The pedestal changed ~6 ADC counts (~1 keV equivalent) while the pedestal -subtracted net output corresponding to the test pulse only changed 1.2 ADC counts (~0.2 keV equivalent). The variation in the pedestal position can be dynamically monitored and compensated. The variation in the gain is small and will not degrade the system response.

D. Triggering and Timing

The triggering thresholds of the special and normal channels for the three ASICs are summarized in Table III. These are the lowest thresholds that the system will not be loop-triggered by itself due to cross-talk noise of the digital control signals. The

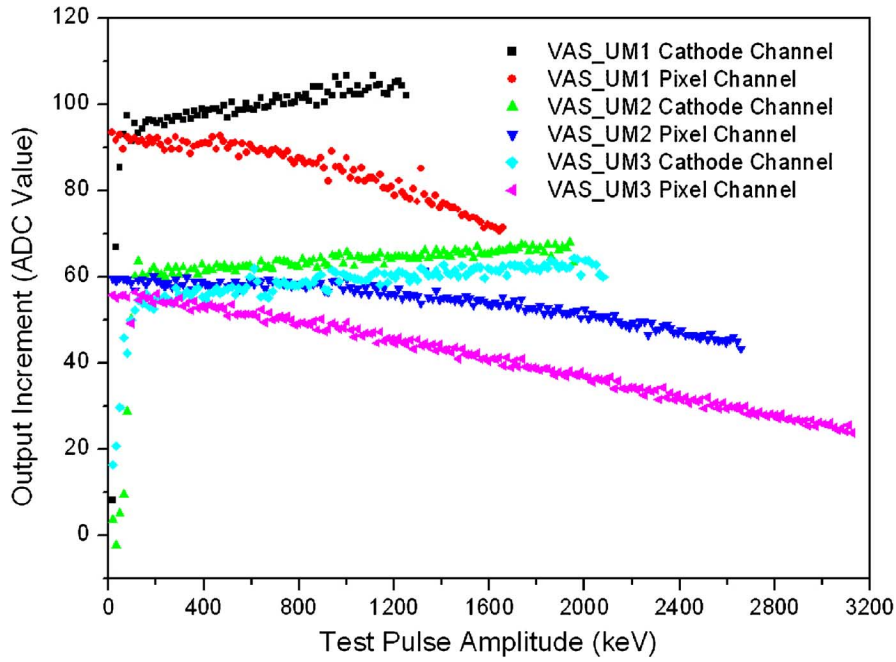

Fig. 8. Linearity of the special channels (cathode) and the normal channels (pixel) for three types of ASICs. The results shown are the increase in the ADC output for each equal increase in the calibration pulse amplitude.

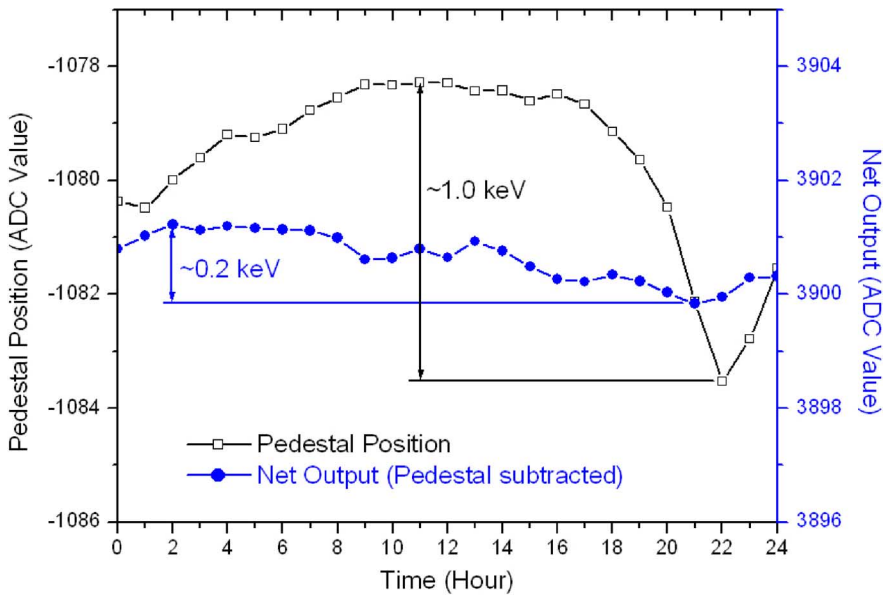

Fig. 9. Pedestal and gain variation during 24 hours experiment time, while the ambient temperature changed $\sim 5^{\circ}$C.

results for the VAS_UM1/TAT4 and VAS_UM2/TAT4 meet the design expectation very well. Further investigation is needed for the VAS_UM3/TAT4 system.

The gain of the timing output was measured to be ~ 1.5 ADC counts per nanosecond (ns) and the noise in the timing signal was ~ 6 ADC counts FWHM. Therefore, the broadening in the timing signal due to electronic noise is only 4 ns FWHM. This is negligible comparing to the normal ~ 500 ns drift time of electrons in a 1-cm thick CdZnTe detector biased at -2000 V.

TABLE III
TRIGGERING THRESHOLDS OF THE SPECIAL CHANNEL AND NORMAL CHANNEL FOR THE THREE TYPES OF ASICS

	VAS_UM1	VAS_UM2	VAS_UM3
Special channel (keV)	25	30	50
Normal channel (keV)	30	40	35

V. Summary

The 4th-generation readout systems based on the VAS_UM/TAT4 ASICs for 3-D position sensitive CdZnTe/HgI_2 detector arrays have been developed and tested. The design of the new ASIC is based on the proven VAS3.1/TAT3 ASIC while focusing on integrating the energy and timing circuits into a single chip, shrinking the size of the ASIC and the front-end board. The whole readout electronics have been designed to be scaleable. This means that multiple detector modules can be plugged in one motherboard to form a detector array, and multiple motherboards can be interconnected to achieve even higher efficiency without sacrificing the energy resolution.

The performances of the three new systems have been evaluated. The test results of the VAS_UM1/TAT4 and the VAS_UM2/TAT4 system meet our expectations very well, while the VAS_UM3/TAT4 needs further investigation. Given the low electronic noise we measured in the VAS_UM1/TAT4 system, we are quite confident that the excellent energy resolution ($<1.0\%$ FWHM at 662 keV) we achieved in the VAS3.1/TAT3 system can be reproduced on the new systems.

The size of the motherboard is still larger than desired for a hand-held device, and an additional digital readout board and a digital I/O card are still required in the current system. Additional design iterations of the ASIC readout system are needed to shrink the entire readout system to closely match the size of the detector array. However, this is the first step towards a compact, high-efficiency and high-resolution CdZnTe spectrometer and imager.

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